6/13/02

Examiner Lewis,

AU 2822

Re: 09/992,387

CP3-B07

Please find attached edited search results from the patent and non-patent commercial abstract and full-text databases. The search strategy was based on the claims and the statements of the technical problems and solutions. Yellow-tagged records might be worth your review.

If you have any further questions, please let me know.

Thanks,

Irina Speckhard

Irina Speckhard
308-6559
STIC-EIC2800
CP4-9C18

EIC2800
Search Results
Feedback Form (Optional)

Scientific & Technical Information Center

The search results generated for your recent request are attached. If you have any questions or comments (compliments or complaints) about the scope or the results of the search, please contact ***the EIC searcher*** who conducted the search ***or contact***:

Jeff Harrison, Team Leader, 306-5429

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* __________ *(Example: 2830)*

- *Relevant prior art found, search results used as follows:*

  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:

  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art* ***not found***:

  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Search results were not useful in determining patentability or understanding the invention.

Other Comments:

Drop off completed forms in **CP4-9C18,** or send to **Jeff Harrison, CP4-9C18.**

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     FILE 'INPADOC, WPIX, HCAPLUS, JAPIO, PATOSEP, PATOSWO' ENTERED AT
     09:52:08 ON 13 JUN 2002
                E JP98-0182942/PRN,AP
L2            3 SEA ABB=ON  PLU=ON  (JP98-182942/PRN OR JP98-182942/AP)
                D ALL TOT

     FILE 'REGISTRY' ENTERED AT 09:56:55 ON 13 JUN 2002
L3            1 SEA ABB=ON  PLU=ON  GOLD/CN
L4            0 SEA ABB=ON  PLU=ON  CU.NI.PD/ELF
L5            1 SEA ABB=ON  PLU=ON  COPPER/CN
L6            1 SEA ABB=ON  PLU=ON  NICKEL/CN
L7            1 SEA ABB=ON  PLU=ON  PALLADIUM/CN
L8           40 SEA ABB=ON  PLU=ON  CU.NI.PD/MF

     FILE 'HCAPLUS' ENTERED AT 09:59:10 ON 13 JUN 2002
L9           30 SEA ABB=ON  PLU=ON  L3(L)BALLS
L10          58 SEA ABB=ON  PLU=ON  L5(L)BALLS
L11          49 SEA ABB=ON  PLU=ON  L6(L)BALLS
L12           9 SEA ABB=ON  PLU=ON  L7(L)BALLS
L13           0 SEA ABB=ON  PLU=ON  L4 AND (BALL OR BGA OR GRID)
L14          16 SEA ABB=ON  PLU=ON  L10 AND L11
L15           2 SEA ABB=ON  PLU=ON  L10 AND L12
L16           3 SEA ABB=ON  PLU=ON  L11 AND L12
L17           2 SEA ABB=ON  PLU=ON  L14 AND L15
                D BIB AB HITSTR 1-2
L18           2 SEA ABB=ON  PLU=ON  L9 AND RESIN
L19           0 SEA ABB=ON  PLU=ON  L9 AND PITCH
L20           3 SEA ABB=ON  PLU=ON  L9 AND FLIP#####
L21           3 SEA ABB=ON  PLU=ON  L9 AND FLIP#########
L22           1 SEA ABB=ON  PLU=ON  (L18 OR L19 OR L20 OR L21) NOT L17
                D BIB AB HITSTR
L23        4906 SEA ABB=ON  PLU=ON  (CU OR COPPER)(3A)(NI OR NICKEL)(3A)(PD OR
                PALLADIUM)
L24          24 SEA ABB=ON  PLU=ON  L23 AND (BALL OR BGA OR FLIP#######)
L25          23 SEA ABB=ON  PLU=ON  L24 NOT (L22 OR L17)
L26           9 SEA ABB=ON  PLU=ON  L25 AND (PITCH#### OR CENTER##### OR
                CENTR##### OR OUTLINE OR MU OR MICRON)
L27           0 SEA ABB=ON  PLU=ON  L25 AND (RESIN#### OR ?IMIDE? OR ?IMIDO?)
                D L26 ALL TOT
L28         175 SEA ABB=ON  PLU=ON  INTERPOS###### AND (BGA OR GRID OR BUMP OR
                BALL)
L29          17 SEA ABB=ON  PLU=ON  L28 AND RESIN
L30           8 SEA ABB=ON  PLU=ON  L29 AND (PITCH#### OR CENTR##### OR
                CENTER##### OR MU OR MICRON OR INTEGRATION)
L31           2 SEA ABB=ON  PLU=ON  L29 AND FLIP#########
L32           8 SEA ABB=ON  PLU=ON  (L30 OR L31)
L33           8 SEA ABB=ON  PLU=ON  L32 NOT (L26 OR L22 OR L17)
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L33 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:882885 HCAPLUS
DN 136:77855
TI Feasibilities on micro-thin underfill technologies for gap less than 10 .**mu**.m applied to **flip**-chip bonding in 20 .**mu**.m **pitch**
AU Tomita, Yoshihiro; Ando, Tatsuya; Tanaka, Naotaka; Sato, Tomotoshi; Takahashi, Kenji
CS Tsukuba Res. Center, Electronics System Integration Technology Research Dept., Association of Super-Advanced Electronics Technologies (ASET), Sengen, Tsukuba-shi, Ibaraki, 305-0047, Japan
SO Erekutoronikusu Jisso Gakkaishi (2001), 4(7), 607-614
CODEN: EJGAF8; ISSN: 1343-9677
PB Erekutoronikusu Jisso Gakkai
DT Journal
LA Japanese
CC 76-3 (Electric Phenomena)
AB The underfill process was examd. to encapsulate the gaps <10 .**mu**.m in thickness between the 10-mm-square Si chips and the **interposer** connected with 12 .**mu**.m **bumps** in 20 .**mu**.m **pitch**. The anal. by the finite element method (FEM) found that the filler particles in an epoxy **resin** were necessary for the relaxation of the thermal stress on the top surface of the 50-.**mu**.m-thickness thin Si chip at the decrease of temp., because the fillers could reduce the thermal stress contraction of the underfill **resin**. Then, the diam. of the filler particles incorporated in an epoxy **resin** at 50% in wt. was optimized as the 0.3 .**mu**.m in av. and 0.35 .**mu**.m in max. for the 3 .**mu**.m gap in thickness. As the results of the expt. on the encapsulation, the optimum filler dispersion could realize the underfill encapsulation for 20-.**mu**.m-**pitch** **flip**-chip interconnections leading to the die-stacked 3-dimensional LSL.
IT Epoxy **resins**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(feasibilities on micro-thin underfill technologies for gap less than 10 .**mu**.m applied to **flip**-chip bonding in 20 .**mu**.m **pitch**)

L33 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:363927 HCAPLUS
DN 136:71114
TI A novel epoxy encapsulant for CSP (.**mu.BGA**) - new hydrophobic epoxy elastomer
AU Xu, Frank Y.; Bymark, Richard; Hsu, Bin-Lin
CS Fiber Optics and Electronic Materials Technology Center, 3M Company, Austin, TX, 78726, USA
SO Proceedings - International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, Braselton, GA, United States, Mar. 6-8, 2000 (2000), 83-89 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 69BHZK
DT Conference
LA English
CC 39-15 (Synthetic Elastomers and Natural Rubber)
Section cross-reference(s): 38, 76
AB Due to an increasing demand for smaller and higher d. packages, Tessera developed .**mu.BGA** technol. as a cost-effective soln. for chip-size packaging. Many companies including Intel, 3M, Samsung, Amkor, etc. have licensed the technol. since 1995. As a current, leading technol. for Chip Scale Packaging (CSP), a .**mu.BGA** package typically has a compliant layer between the die and the flex **interposer** to eliminate strain on solder **balls** by thermal mismatch of the die and printed wire board (PWB). Historically, a silicone-based encapsulant has been the material of choice for this application. However, for hard disk drive and other applications with zero tolerance of siloxane outgassing, a non-silicone encapsulant having excellent reliability performance is highly desired. A novel 3M epoxy encapsulant with excellent hydrophobicity has been developed for an advanced .**mu.BGA** package platform. The new epoxy encapsulant is designed to meet the requirements of compliancy with good moisture resistance. This new material has demonstrated JEDEC level 1 reliability. During thermal cycling tests, the new encapsulant far surpassed 1000 cycles, both on- and off-board, and survived high temp. aging, as well as 500 h of pressure cooker testing (PCT). This paper will describe phys. properties and reliability performances of the new 3M encapsulant material with emphasis on its hydrophobicity and compliancy. Improvement in reliability trends for .**mu.BGA** technol. will also be discussed.
IT Epoxy **resins,** properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(rubber; novel hydrophobic elastomeric epoxy encapsulant for chip scale packaging applications)

L33 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:40380 HCAPLUS
TI Semiconductor device package for suppressing warping in semiconductor chips
IN Morifuji, Tadahiro
PA Rohm Co., Ltd., Japan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L023-48
ICS H01L023-52; H01L023-40
NCL 257777000
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6175157	B1	20010116	US 1998-45135	19980320
PRAI	JP 1997-68540	A	19970321		

AB A semiconductor device includes a main chip and a sub-chip. The both chips are in a mount-structure, and molded by a **resin** package. The main chip has electrode pads formed at an periphery in a connecting surface thereof, while the sub-chip has a plurality of connecting **bumps** formed at a periphery in a connecting surface at positions corresponding to the plurality of electrode pads. A plurality of dummy **bumps** are formed at a **central** area of the connecting surface of the sub-chip. Connections are made respectively between the connecting **bumps** and the connecting electrodes. The main chip and the sub-chip have the connecting **bumps** and dummy **bumps interposed** therebetween to thereby prevent the main chip and/or the sub-chip from warping.

L33 ANSWER 4 OF 8 HCAPLUS

AN 2000:495313 HCAPLUS
DN 133:230723
TI The key role of dielectric materials for advanced interconnect solutions
AU Meier, Martin B.; Achen, Albert
CS Dow Europe S.A., Horgen, Switz.
SO Produktion von Leiterplatten und Systemen (2000), 2(6), 972-978
CODEN: PLSYF3; ISSN: 1436-7505
PB Eugen G. Leuze Verlag
DT Journal; General Review
LA English
CC 76-0 (Electric Phenomena)
Section cross-reference(s): 38

AB Global market trends and future needs for specific semiconductor markets are reviewed with 10 refs. The dielec. material is a key element for advanced interconnect due to reduced feature sizes and **integration** aspects with other elements such as metals, solder **bumps**, adhesives, etc. New dielec. materials such as CYCLOTENE* advanced electronic **resins** (BCB) or SiLK* semiconductor dielec. were developed to meet today's and future needs. The key parameters of BCB and its benefits for applications such as on chip interconnect, CSP/redistribution, device passivation, high d. **interposer** or **BGAs**, HDI- or RCC-type substrates, MCMs and optical interconnect are presented.

L33 ANSWER 5 OF 8 HCAPLUS
AN 1999:609047 HCAPLUS
DN 131:330576
TI Packaging properties of ALIVH-CSP using SBB **flip**-chip bonding technology
AU Itagaki, Minehiro; Amami, Kazuyoshi; Tomura, Yoshihiro; Yuhaku, Satoru; Ishimaru, Yukihiro; Bessho, Yoshihiro; Eda, Kazuo; Ishida, Toru
CS Device Engineering Development Center, Matsushita Electric Industrial Co., Ltd., Osaka, 571-8501, Japan
SO IEEE Transactions on Advanced Packaging (1999), 22(3), 366-371
CODEN: ITAPFZ; ISSN: 1521-3323
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB A new chip scale package (CSP) using an org. laminated substrate called . **mu**.CSP was developed, which was fabricated using ALIVH substrate as a **interposer** and stud-**bump**-bonding (SBB) **flip**-chip technol. The ALIVH substrate is a multilayered org. substrate with inner via holes in any layer. The newly developed CSP-L using ALIVH substrate had realized a miniaturization of its package size same as a CSP using a ceramic substrate (CSP-C). To perform the SBB **flip**-chip bonding onto the ALIVH substrate, an excellent coplanarity of the substrate surface was required. The required coplanarity was obtained using a fixture during the SBB **flip** -chip bonding process. The 1st-level packaging reliability and the 2nd-level packaging reliability onto ALIVH mother board were evaluated. The resulting reliabilities were good enough to apply to the practical use.

L17 ANSWER 1 OF 2 HCAPLUS
AN 1997:34175 HCAPLUS
DN 126:83213
TI Semiconductor device with solder bumps with resin balls for flip-chip bonding
IN Komura, Atsushi
PA Citizen Watch Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08288291	A2	19961101	JP 1995-92260	19950418

AB The device is packaged by flip-chip bonding which contacts elec. contacts of a semiconductor chip and a pad on a wiring substrate via solder bumps including resin ball cores. The resin balls may be coated with Au, SnPb, Pd, Ni, or Cu by electroless plating. The device shows high reliability of its contacts preventing crack generation in the solder bumps.
IT **7440-02-0**, Nickel, uses **7440-05-3**, Palladium, uses **7440-50-8**, Copper, uses
RL: DEV (Device component use); USES (Uses)
(resin ball coating; semiconductor device with solder bumps with resin **balls** for flip-chip bonding)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-05-3 HCAPLUS
CN Palladium (8CI, 9CI) (CA INDEX NAME)

Pd

RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

L17 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:609504 HCAPLUS
DN 125:236295
TI Semiconductor chip bonding and bonding balls
IN Hayashida, Hidenori; Tsucha, Shoji
PA World Metal Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08191073	A2	19960723	JP 1995-67116	19950228
PRAI	JP 1994-302905		19941110		

AB The balls comprise micrograins chem. plated with Pd (alloy). The micrograins may be metals, resins, ceramics, or glasses. The Pd plating layer may further be coated with a metal layer which lowers the melting temp. of the plating. The methods using the balls are claimed for flip-chip method and BAG (ball grid array) method.
IT **7440-02-0**, Nickel, processes **7440-50-8**, Copper, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in semiconductor chip bonding by Pd-plated bonding **balls**)
RN 7440-02-0 HCAPLUS
CN Nickel (8CI, 9CI) (CA INDEX NAME)

Ni

RN 7440-50-8 HCAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

IT **7440-05-3**, Palladium, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(semiconductor chip bonding and Pd-plated bonding **balls**)
RN 7440-05-3 HCAPLUS
CN Palladium (8CI, 9CI) (CA INDEX NAME)

Pd

L22 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:251972 HCAPLUS
DN 136:266676
TI Filled solder balls with adjusted thermal expansion for **flip** -chip packages and thermal contacts
IN Koning, Paul A.
PA Intel Corporation, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6365973	B1	20020402	US 1999-457057	19991207

AB A filled solder material comprising a solder material having a plurality of coated filler particles disposed therein, wherein said coated filler particles alter the coeff. of thermal expansion of the filled solder material. The coated filler particles are preferably made of a low CTE material, such as graphite, carbon fiber, diamond, boron nitride, aluminum nitride, silicon carbide, silicon nitride, zinc oxide, alumina, titanium diboride, and silica, with a coating which is wettable with the solder material, such as cobalt, copper, copper oxide, nickel, iron, tin, tin oxide, zinc, and alloys thereof. The solder material may include Sn, Pb, In, Ga, Bi, Cd, Zn, Cu, Au, Ag, Sb, Ge, and alloys thereof. In application, the filler solder material may be used as an elec. contact, such as solder balls on a **flip**-chip package, as a thermal contact, such as an attachment material between a microelectronic chip and a heat dissipation device, and/or as a mech. attachment mechanism.
IT **7440-57-5**, Gold, uses
RL: MOA (Modifier or additive use); USES (Uses)
(solder alloy component; filled solder **balls** with adjusted thermal expansion for **flip**-chip packages and thermal contacts)
RN 7440-57-5 HCAPLUS
CN Gold (8CI, 9CI) (CA INDEX NAME)

Au

L26 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:22747 HCAPLUS
DN 134:200907
TI Eutectic Sn-Ag solder bump process for ULSI **flip**-chip technology
AU Ezawa, Hirokazu; Miyata, Masahiro; Honma, Soichi; Inoue, Hiroaki; Tokuoka, Tsuyoshi; Yoshioka, Junichiro; Tsujimura, Manabu
CS Advanced Process Engineering Department, Toshiba Corporation Semiconductor Company, Yokohama, 235-8522, Japan
SO Proceedings - Electronic Components & Technology Conference (2000), 50th, 1095-1100
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-2 (Electric Phenomena)
AB The newly developed Sn-Ag eutectic solder bump process provides several advantages over conventional solder bump process schemes. Steep wall bumps as plated were fabricated using a nega-type photoresist with a thickness of more than 50 **.mu.**m by one time spin coating. This improves productivity for mass prodn. The 2-step electroplating process was performed using sep. plating reactors for the Ag and Sn. The eutectic Sn-Ag alloy bumps were easily obtained by annealing the metal stacks with Sn layer on Ag layer sequentially electroplated. This electroplating process does not need strict control of the content ratio of Ag to Sn in an alloy plating soln. even with increasing electroplating depositions. The novel developed process gives the within-wafer uniformity of the bump height as reflowed of less than 10% and of the Sn-Ag alloy compn. as reflowed of less than .+-.0.5 wt.% Ag, analyzed by ICP spectrometry. Shear strength measurements were performed to know the thermal stability for the structure of **Cu** pads/Ti/**Ni**/**Pd**/Sn-Ag eutectic solder stack. In the case of Ti (100 nm)/Ni (300 nm)/Pd (50 nm) barrier metal stacks, the shear strength after 5 times annealing in a N2 ambience at 260.degree. decreased to 70% than that as reflowed. As the Ti becomes thicker in the Ti/Ni/Pd metal stack, shear strengths are improved. Comparing the structure of **Cu**/Ti/**Ni**/**Pd**/Sn-Ag eutectic solder with those of Ta/Ti/Ni/Pd and Nb/Ti/Ni/Pd barrier metal stacks, the anal. results of Auger spectrometry show that Sn diffusion into Cu to form Cu-Sn alloy was obsd. only in **Cu**/Ta/Ti/**Ni**/**Pd** barrier metal stacks. These results suggest that the same Ti/Ni/Pd barrier metal stack as used in Sn-Pb solder bump and Au bump is viable for ULSIs with Cu interconnects.
IT Bump contacts
IT Semiconductor devices
(**flip** chips; eutectic Sn-Ag solder bump process for ULSI **flip**-chip technol.)

L26 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:313359 HCAPLUS
DN 131:76862
TI Studies on the interfacial reaction between electroplated eutectic Pb/Sn **flip**-chip solder bump and UBM (under bump metallurgy)
AU Jang, Se-Young; Paik, Kyung-Wook
CS Dep. of Mater. Sci. and Eng., Korea Advanced Inst. of Sci. and Technol., Taejon, 305-701, S. Korea
SO Han'guk Chaelyo Hakhoechi (1999), 9(3), 288-294
CODEN: HCHAEU; ISSN: 1225-0562
PB Materials Research Society of Korea
DT Journal
LA Korean
CC 56-9 (Nonferrous Metals and Alloys)
Section cross-reference(s): 76
AB In the **flip** chip interconnection using solder bumps, the Under Bump Metallurgy (UBM) is required to perform multiple functions in its conversion of an Al bond pad to a solderable surface. In this study, various UBM systems such as Al1.**mu**.m/Ti0.2.**mu**.m/Cu5. **mu**.m, Al1.**mu**.m/Ti0.2.**mu**.m/Cu1.**mu**.m, Al1.**mu**.m/Ni0.2.**mu**.m/Cu1.**mu**.m and Al1. **mu**.m/Pd0.2.**mu**.m/Cu1.**mu**.m for **flip** chip interconnection using the low m.p. eutectic 63Sn-37Pb solder were investigated and compared to their metallurgical properties. 100 . **mu**.M size bumps were prepd. using an electroplating process. The effects of the no. of reflows and aging time on the growth of intermetallic compds. (IMC) were investigated. Cu6Sn5 and Cu3Sn IMC were obsd. after aging treatment in the UBM system with thick copper (Al 1 . **mu**.m/Ti 0.2 .**mu**.m/Cu 5 .**mu**.m). However only the Cu6Sn5 was detected in the UBM systems with 1 .**mu**.m thick Cu even after 2 reflows and 7 day aging at 150.degree.C. Complete Cu consumption by Cu-Sn IMC growth gives rise to a direct contact between solder inner layer such as Ti, Ni, and Pd, and hence to possibly cause reactions between two of them. In this study, however, only for the Pd case, IMC of PdSn4 was obsd. by Cu consumption. UBM interfacial reactions with solder affected the adhesion strength of solder **balls** after solder reflow and annealing treatment.
T 7429-90-5, Aluminum, processes 7440-02-0, Nickel, processes 7440-05-3, Palladium, processes 7440-32-6, Titanium, processes 7440-50-8, Copper, processes
RL: PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process)
(interfacial reaction between electroplated eutectic Pb/Sn **flip** -chip solder bump and under-bump metallurgies contg. Al, **Cu**, **Ni**, **Pd**, and Ti layers)

L26 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:643443 HCAPLUS
DN 125:290779
TI Bump electrode or pad electrode for external contact and its formation
IN Watanabe, Eiji; Makino, Yutaka; Yoda, Hiroyuki; Nagae, Kenichi
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-321
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08203907	A2	19960809	JP 1995-12253	19950130

AB The electrode consists of a porous Al2O3 coating contacting an external electrode of a wiring layer formed on a substrate, a good conductor in the pores (e.g., 1/2 of pore depth .ltoreq. conductor thickness .ltoreq. pore depth), an undercoating conductive layer (e.g., **Ni**, **Cu**, **Pd**, or **Pd**-Sn-Pb electroless plating layer with thickness 0.5-5 .**mu**.m), and a bump or pad electrode-forming conductive layer. An Al-based wiring layer, directly contacting the Al2O3 coating, may be formed on a semiconductor substrate or a Cu wiring layer, contacting the Al2O3 coating via an Al-based layer (not oxidized), may be formed on a packaging substrate. An oxidn.-preventing conductive layer may be formed between the undercoating layer and the electrode-forming layer. The process involves deposition of an Al-based layer over an external electrode of a wiring layer, anodic oxidn. of the Al-based layer, electrodeposition of a good conductor in the pores of the Al2O3 film, and electroless plating (e.g., Ni-P or Ni-B plating) of an undercoating layer, and forming the electrode (e.g., with a solder **ball**).
IT 7440-02-0P, Nickel, uses 7440-05-3P, Palladium, uses 7440-50-8P, Copper, uses 182497-76-3P
RL: DEV (Device component use); IMF (Industrial manufacture); PREP (Preparation); USES (Uses)
(undercoatings, electroless plating of; bump electrodes or pad electrodes for semiconductor devices and their formation)

L26 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:124124 HCAPLUS
DN 124:191478
TI Fabrication of bump electrodes on **flip**-chip semiconductor devices
IN Kondo, Ichiji; Tera, Akinosuke; Ito, Motoki; Watanabe, Jusuke; Tanaka, Kazuo; Niimi, Akihiro
PA Nippon Denso Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-321
ICS H01L021-28
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07321116	A2	19951208	JP 1994-131358	19940519

AB The bump electrode, formed on a TiN barrier layer, has a small root diam. of .gtoreq.30 **.mu**.m and mech. strength. The fabrication process involves forming a metal layer, a TiN barrier layer, and an undercoating layer (e.g., **Cu**, **Pd**, **Ni**, Au, **Ni**-Au, **Pd**-Au, W-Cu laminate) on a contact hole of a **flip** chip and forming a bump electrode by electroplating using the undercoating layer.
IT 7440-02-0P, Nickel, uses 7440-05-3P, Palladium, uses 7440-50-8P, Copper, uses 7440-57-5P, Gold, uses
RL: DEV (Device component use); PNU (Preparation, unclassified); PREP (Preparation); USES (Uses)
(bump electrode; fabrication of bump electrodes on **flip**-chip semiconductor devices)